

FIG. 1 is a block diagram of a video processing system. The system includes an input picture 101, an input clock 102, a video input interface 103, an encoding unit 106, a controller 105, a reference time generator 104, and a reordering memory 107. The input picture 101 and input clock 102 are provided to the video input interface 103. The video input interface 103 is connected to the encoding unit 106 and the controller 105. The encoding unit 106 is connected to the reordering memory 107 and the output bit stream 108. The controller 105 is connected to the reference time generator 104 and the encoding unit 106. The reference time generator 104 provides a reference time signal 110 to the controller 105. The controller 105 provides control signals 111, 112, 113, 114, 115, and 118 to the video input interface 103 and the encoding unit 106. The reordering memory 107 is connected to the encoding unit 106 and the output bit stream 108. The output bit stream 108 is provided to the encoding unit 106.

Fig.1

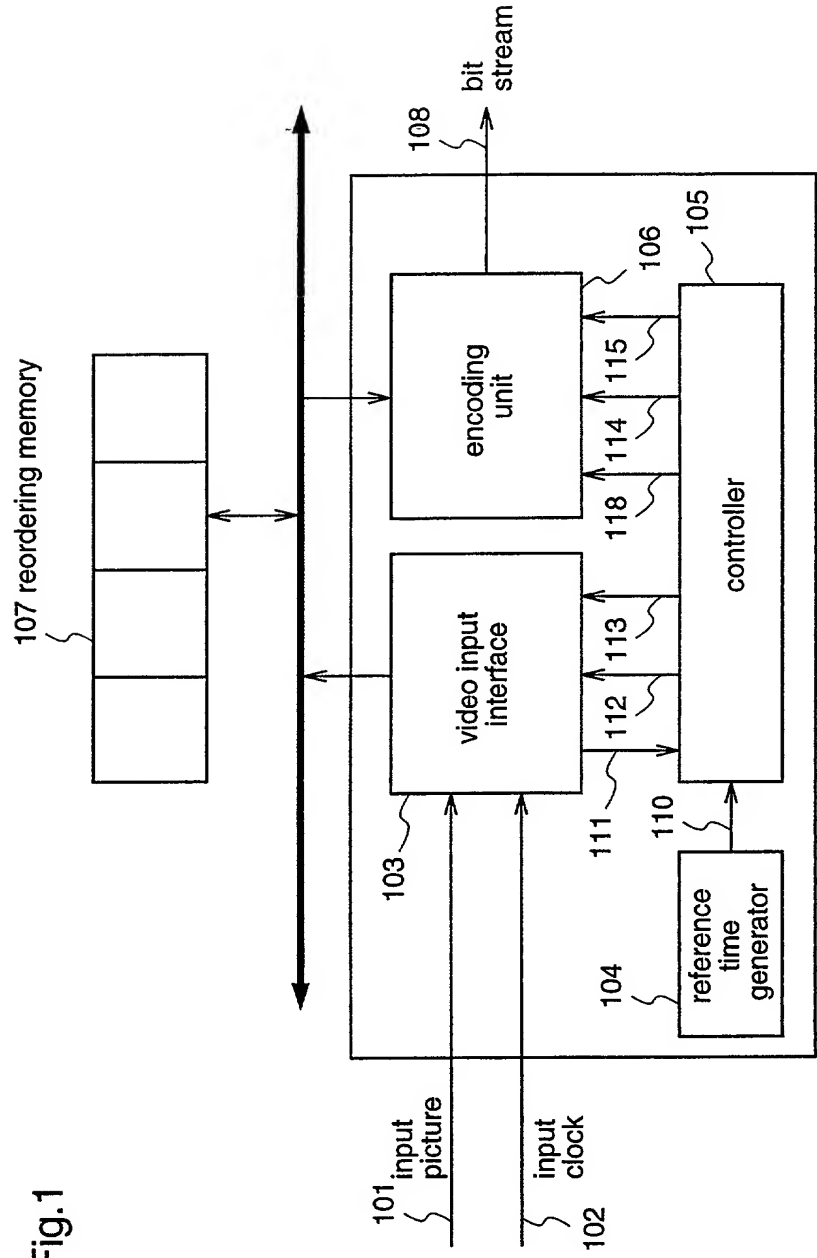


Fig.2

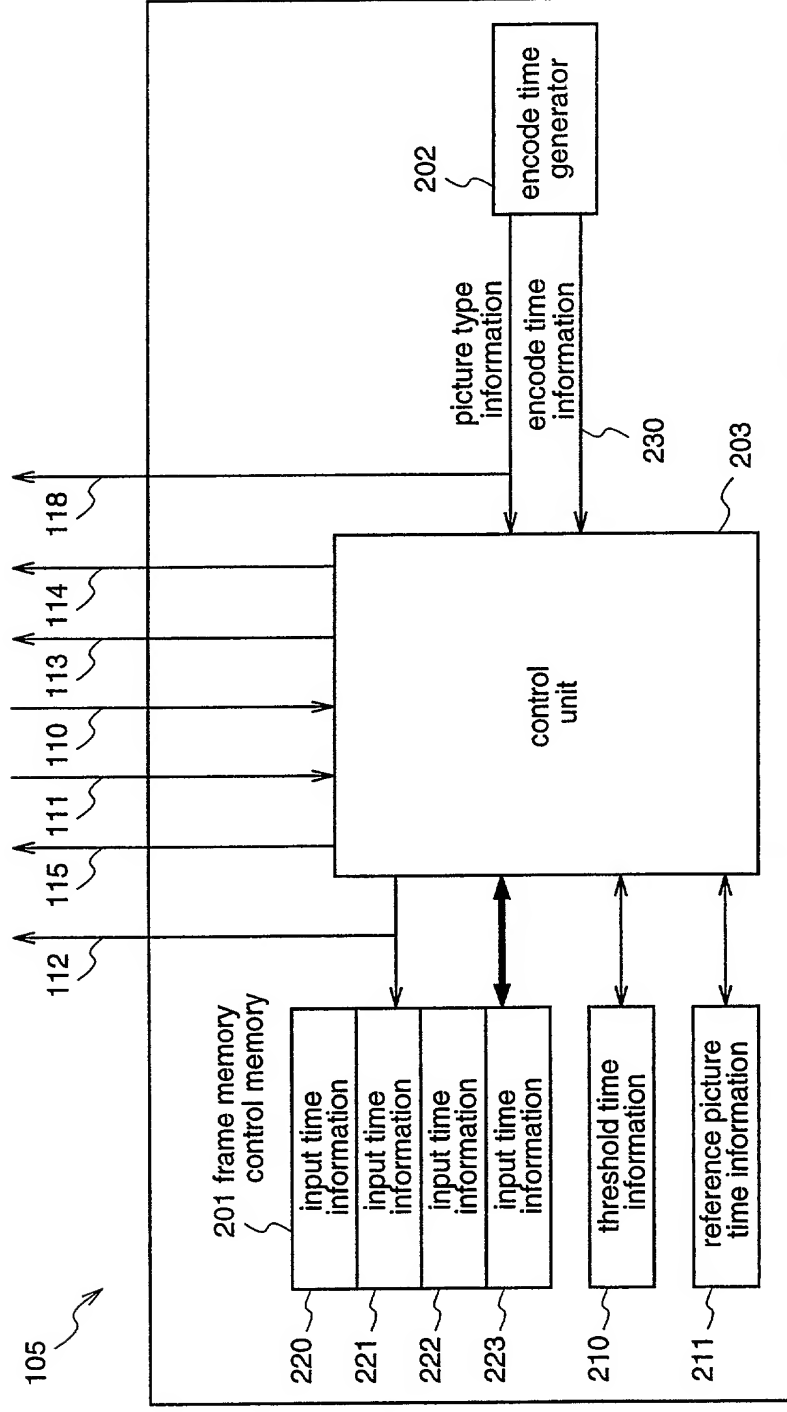


Fig.3

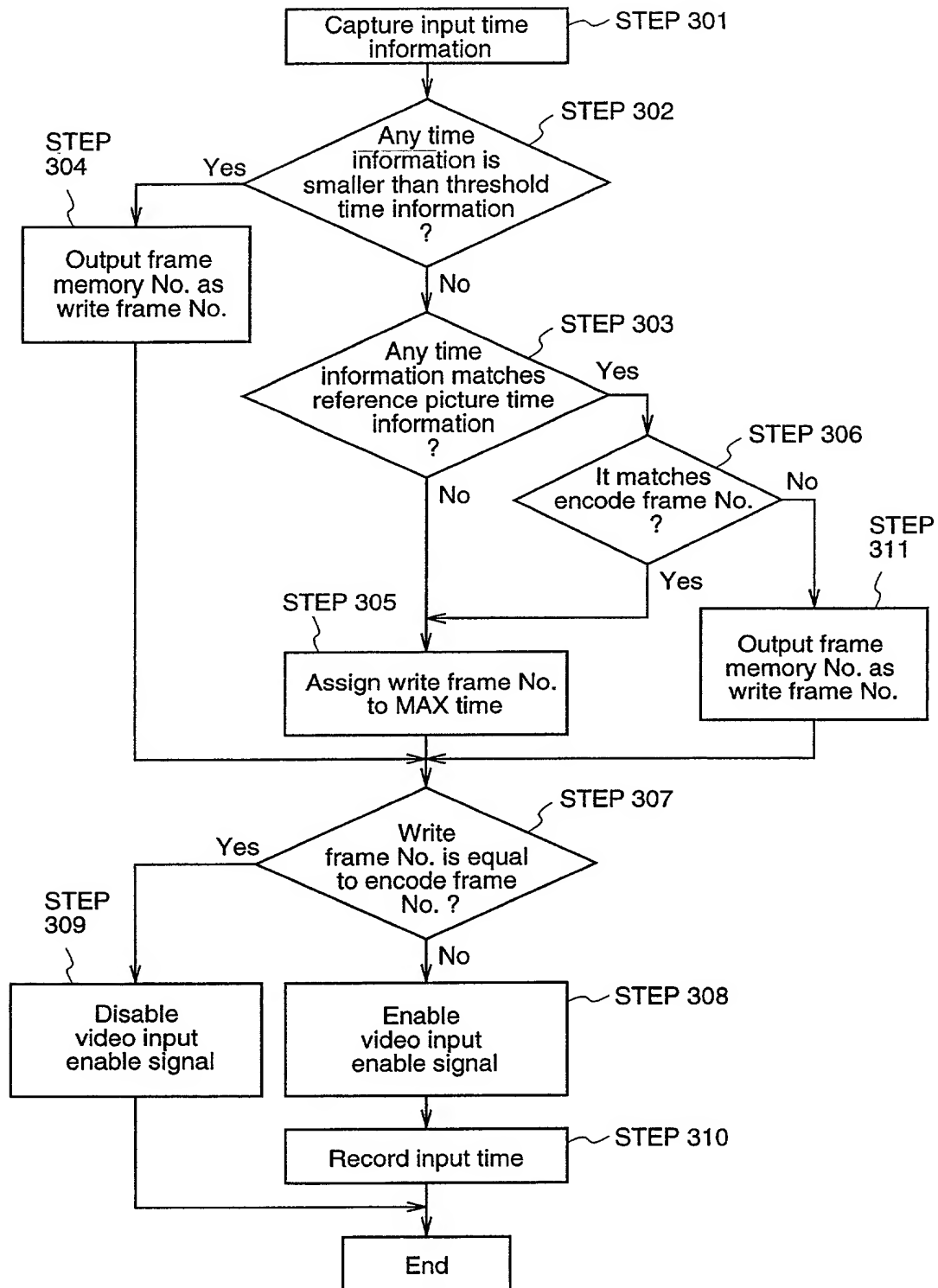


Fig.4

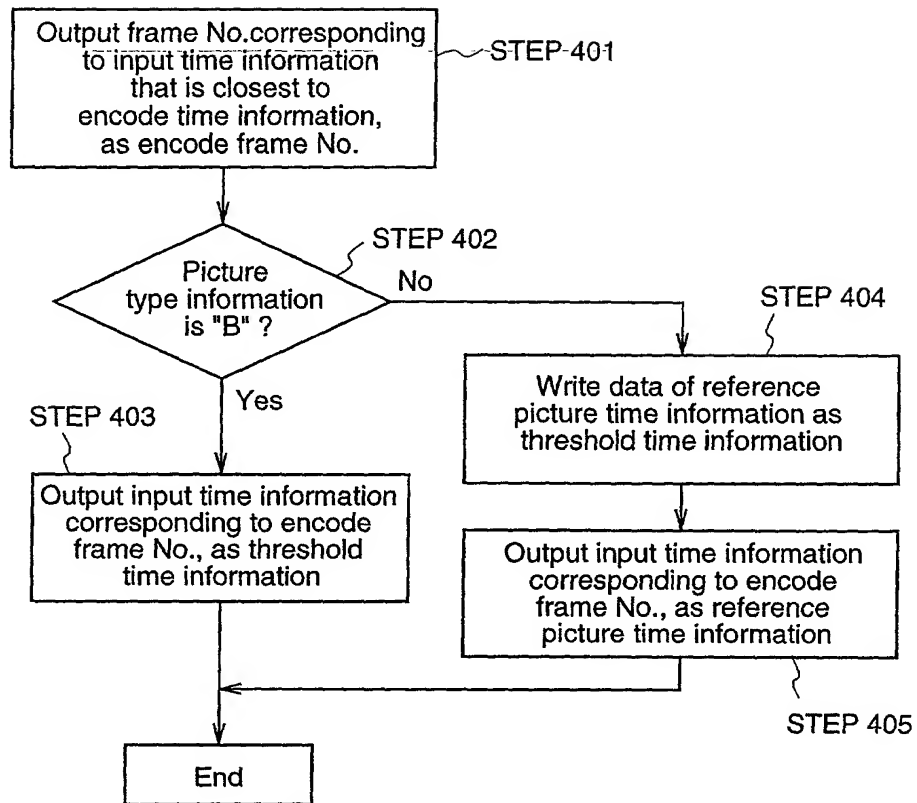


Fig.5

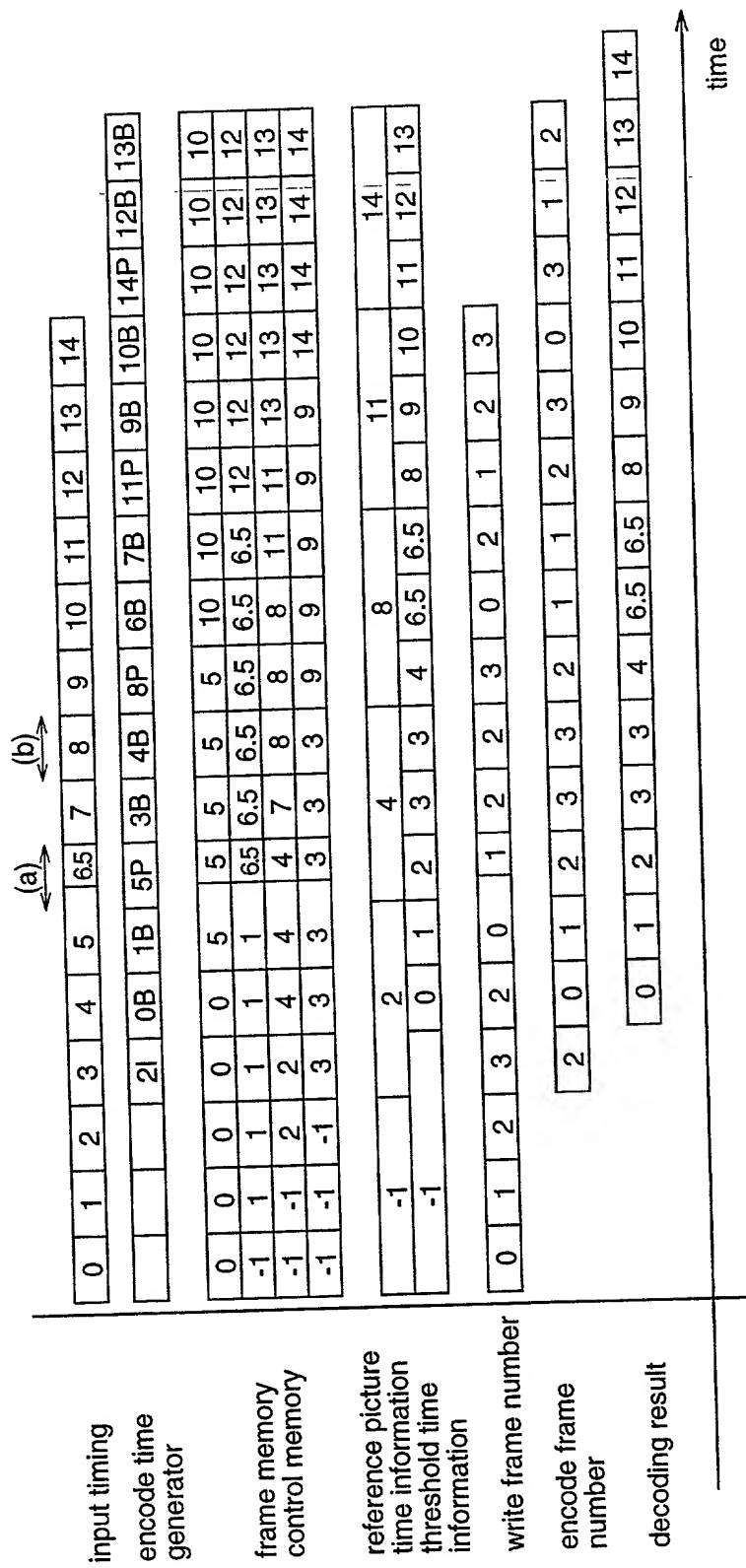


Fig.6

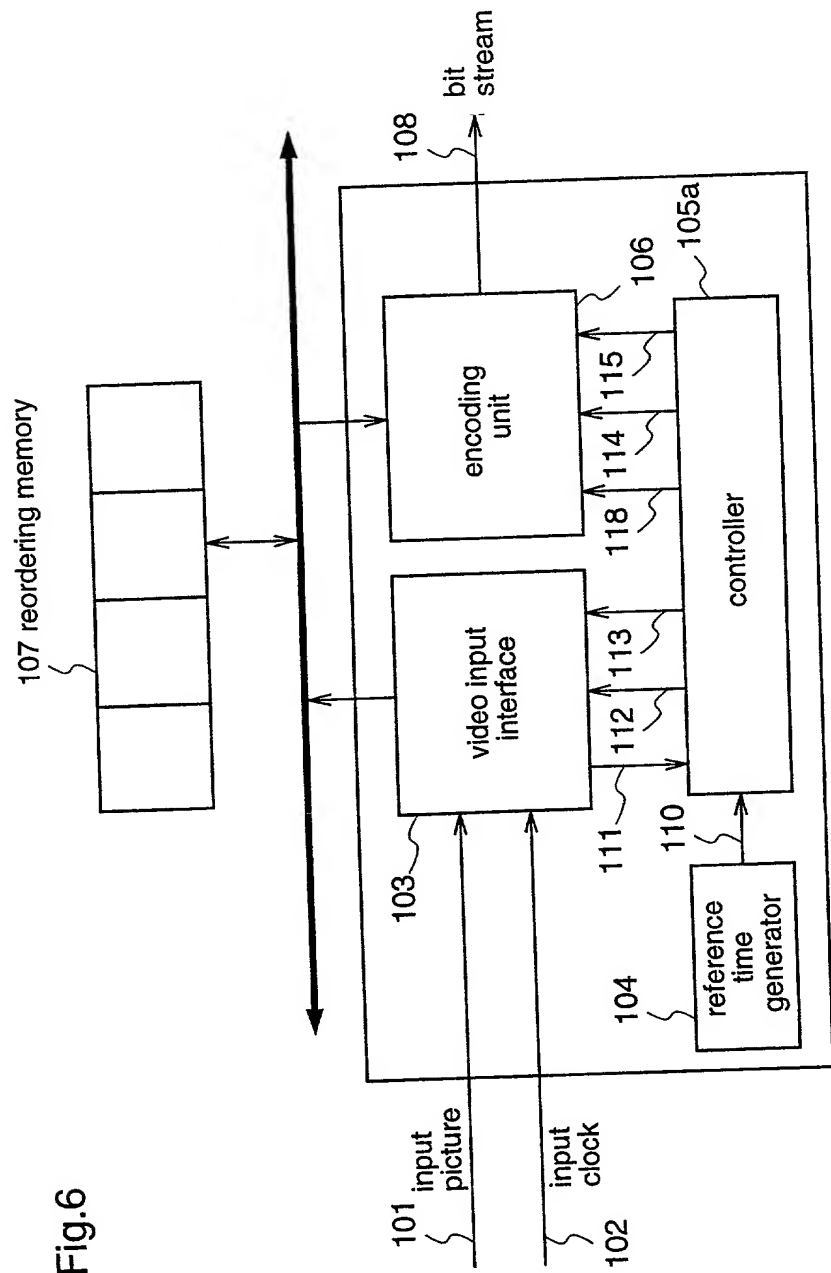


Fig.7

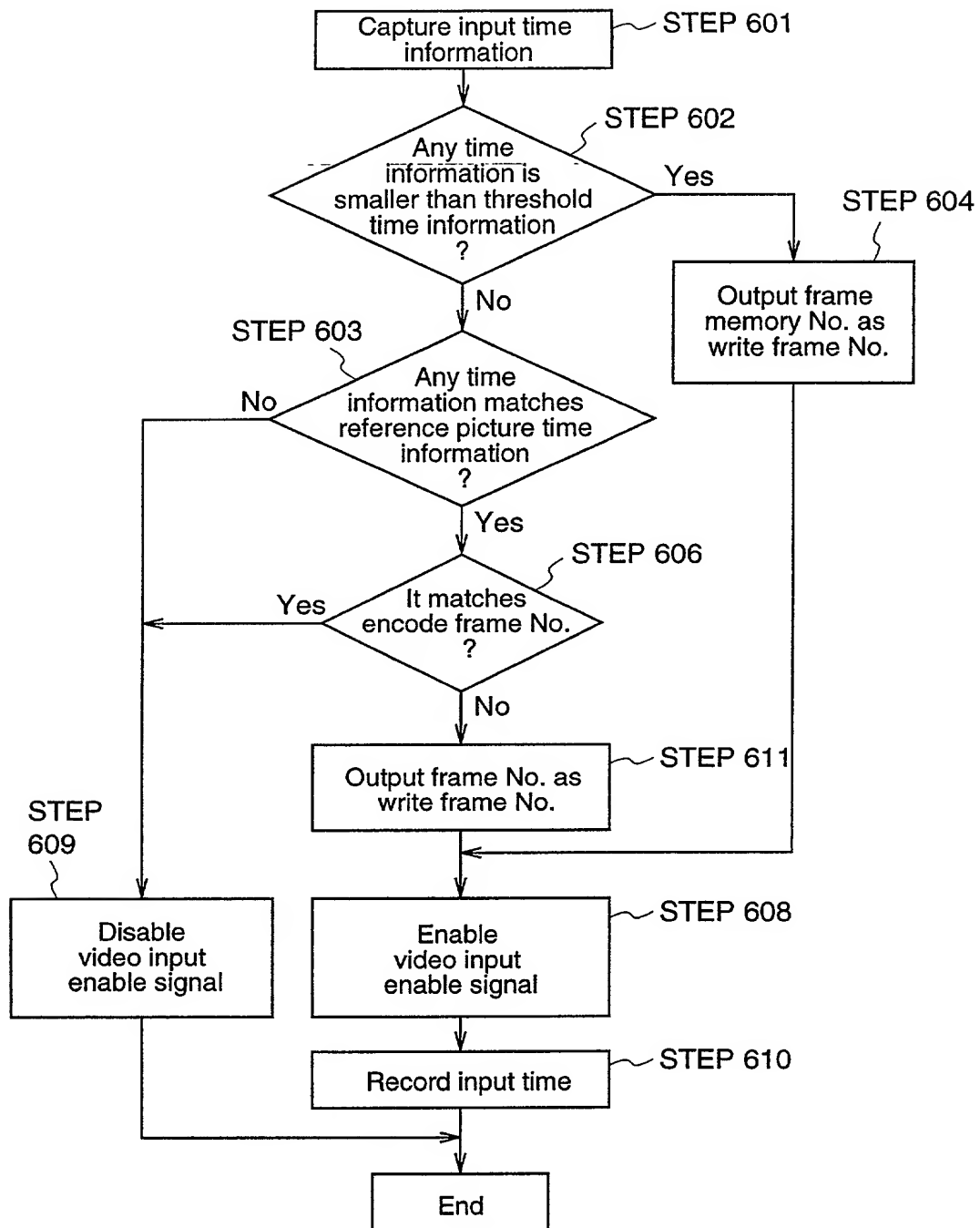


Fig.8

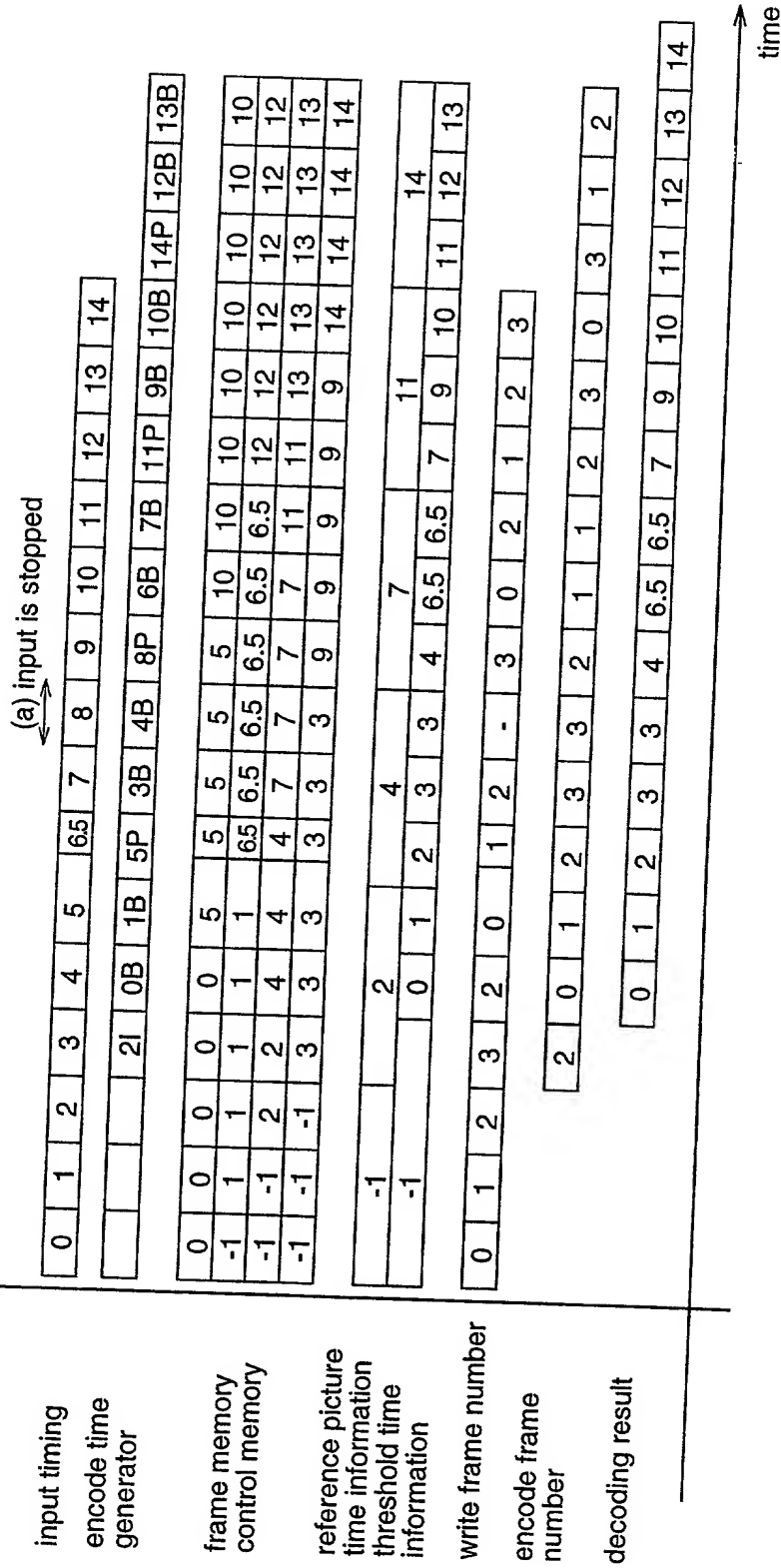




Fig.9

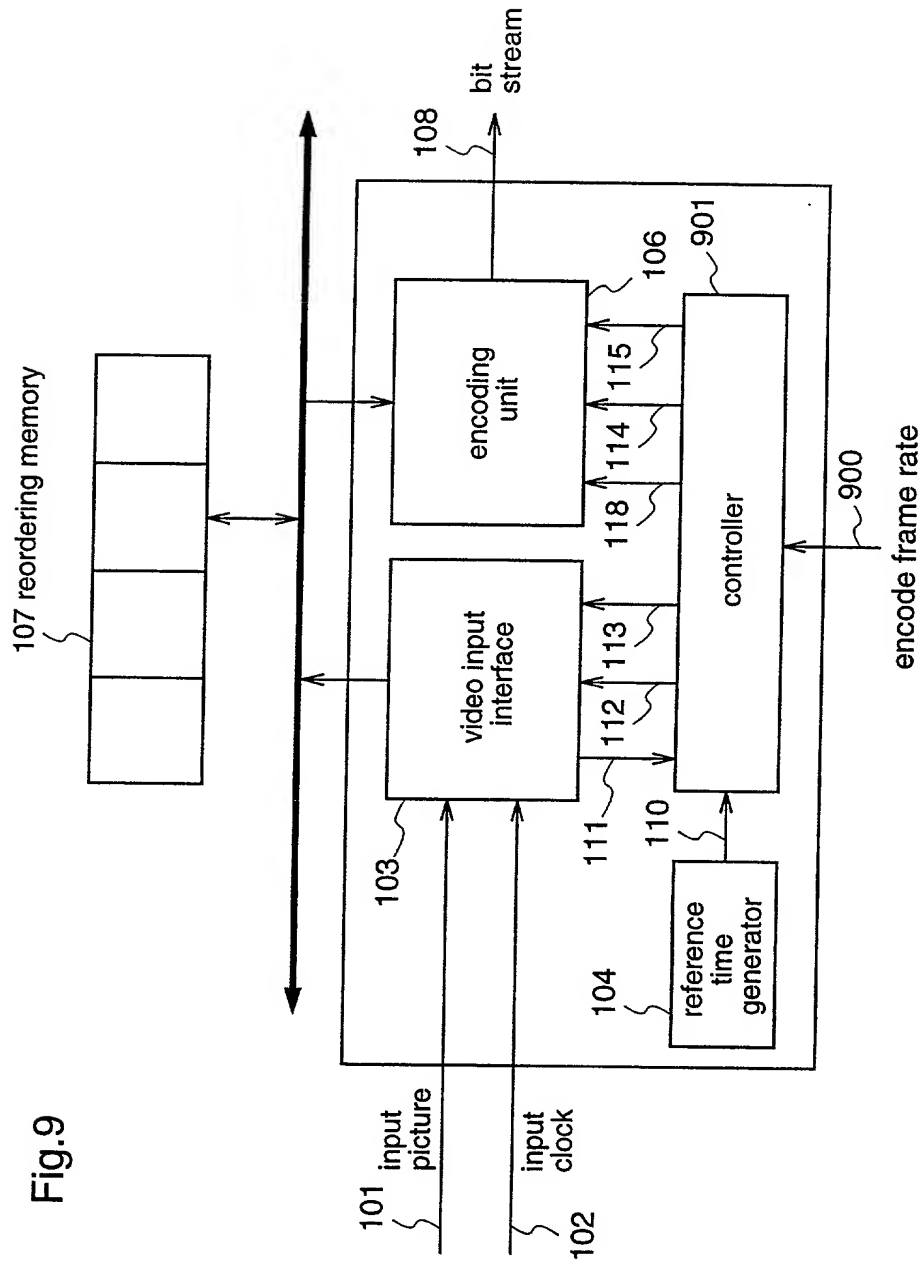


Fig.10

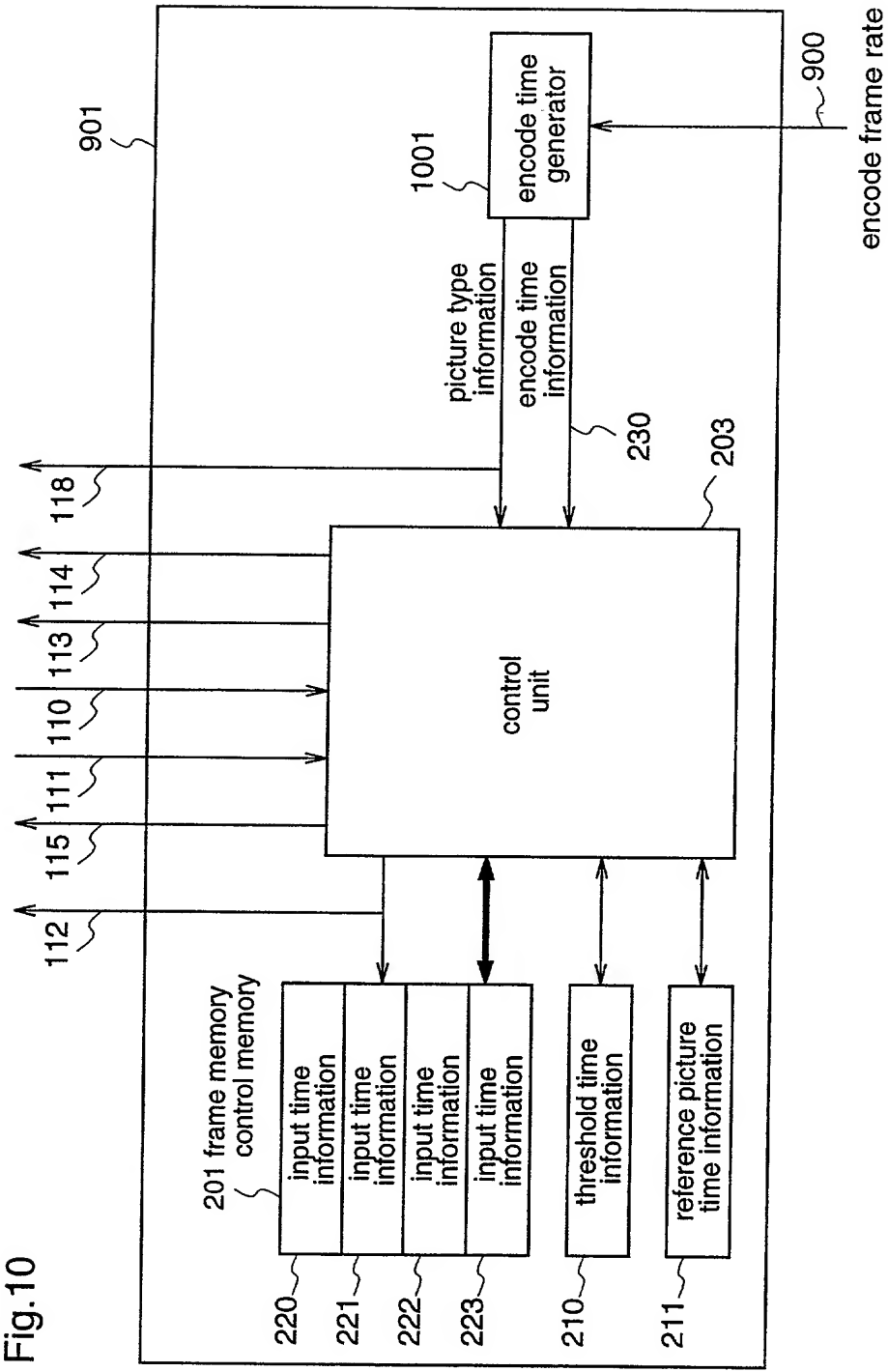


Fig.11

